

REMARKS

After entry of this Amendment, claims 1-21 are pending in this application. Claims 5, 7, and 16 are amended without introduction of new matter. Non-limiting support for the amended language is self-evident or evident from the discussion below.

Figures 1-4 stand objected as being described within the "Background of the Invention" but having no indication of being prior art. In view of the Examiner's comments, Figures 1-4 are labeled "Prior Art". Accordingly, Applicant respectfully requests that this objection be withdrawn.

The specification stands objected as incorporating essential material by reference to a non-U.S. patent or published application. Specifically, the Examiner asserts that the attempt to incorporate Steven R. Norsworthy, Richard Schreies, Gabor Temes, "Delta Sigma Data Converters, Theory, Design, and Stimulation" IEEE press (ISBN 0-7803-1045-4) is ineffective because the subject matter shown in Figure 7 is related to the claimed invention. However, Figure 7 itself is part of the present application and is stated to represent known "Multiple feedback (MFB) filter architectures". As such, neither Figure 7 nor Figure 10.24 of the reference (to which Figure 7 is stated to correspond) constitute "essential material" under 37 C.F.R. 1.57(c).

Applicant respectfully submits that none of the incorporated material is "essential material" as defined by 37 C.F.R. 1.57(c). Accordingly, Applicant respectfully requests that this objection be withdrawn.

The specification also stands objected as failing to refer back to Figure 6 after a discussion of Figure 7. The specification is amended in view of the Examiner's comments. Accordingly, Applicant respectfully requests that this objection be withdrawn.

Claims 5 and 7 stand objected because of informalities. The claims are amended in view of the Examiner's comments. Accordingly, Applicant respectfully requests that this objection be withdrawn.

Claims 16 and 18-20 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. The claims are amended in view of the Examiner's comments. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

Claims 1 and 7 stand rejected under 35 U.S.C. 102(b) as being anticipated by Magrath et al., "Design and Implementation of a FPGA Sigma-Delta Power DAC" (hereinafter "Magrath"). Reconsideration is respectfully requested.

Claim 1 recites: "A bit-flipping sigma-delta modulator for a class D amplifier and comprising: a quantiser coupled to a bit-flipping means; one or more look-ahead quantisers; and a controller having inputs from the quantiser and the look-ahead quantiser and arranged to enable the bit-flipping means to provide a different output from that of the quantiser in order to reduce the quantised output transition rate of the modulator; a feedback circuit arranged to add a portion of the quantiser output to the input signal path of the modulator, and further comprising an integrator circuit in the input signal path between the input and the quantiser, the integrator circuit having a compensation circuit for adjusting the input to the quantiser when said previous modulator output has been changed by the bit flipping means from said previous quantiser output." The remaining rejected claims depend directly or indirectly from claim 1.

The outstanding Office Action cites Magrath's "integrator with mux in fig. 4" as teaching the recited integrator. Magrath's Figure 4 is shown below. As can be seen, the "integrator with mux in fig. 4" is arranged after the quantizer, and not "in the input signal path between the input and the quantiser", as claimed. Thus, as the cited reference does not teach each and every recited element as arranged, this rejection under 35 U.S.C. §102 is improper.

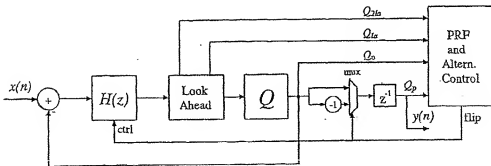


Figure 4: Complete Block Diagram of BF-SDM.

Applicant further notes that the recited arrangement of the integrator “in the input signal path between the input and the quantiser” has at least one advantage that should be considered in determining the patentability of the claimed invention under 35 U.S.C. §103. As explained with reference to Applicant’s Figures 6a-c, which provide a non-limiting example of this recited arrangement:

In the case where bit flipping does occur, the quantizer output with respect to the loop changes state, and so the loop must be modified to respond correctly. ... In particular, whilst the $-b$ or $+b$ coefficient added by adder A_0 is correct for the feedback loop for Q_{1a} , it is incorrect for feedback for Q ; and so is corrected by adding $2b_0$ or subtracting $(-)2b_0$ to remove the $-b_0$ or b_0 coefficient **from the input to Q** . This is achieved by multiplier M_10 selecting adder A_{1a0} [shown in integrator I_{1a0} of Figure 6b].

US 2005/0058209, para. 95 (emphasis added).

Accordingly, for at least the above-stated reasons, Applicant respectfully requests that this rejection be withdrawn.

Claim 21 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Magrath because, according to the Office Action, “[A class D amplifier as in claim 1] for implementing a Delta-Sigma Modulation is widely and notoriously known for converting the received high bit rates bits to high frequency low bit rate and Examiner is taken an official notice.” In response, Applicant respectfully submits that, regardless of whether it is known to use class D amplifiers for implementing sigma delta modulation, the subject matter of the particular class D amplifier of claim 1, from which claim 21 depends, would not have been obvious for the reasons set forth above. Accordingly, in view of the remarks provided with respect claim 1, Applicant respectfully requests that this rejection be withdrawn.

As all issues are believed to be addressed by this Amendment, Applicant respectfully requests that the claims be allowed and this application passed to issue.

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Respectfully submitted, _

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